PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

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Applicant's or agent's file reference	FOR FURTHER ACTION	See Form PCT/IPEA/416
P10003WO/PDGW		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/GB2004/005053	02.12.2004	03.12.2003
International Patent Classification (IPC) or national classification and IPC		
INV. G06F17/50		
Applicant		
SYMGENIS LIMITED		

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 5 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. ☒ *sent to the applicant and to the International Bureau)* a total of 3 sheets, as follows:
      ☒ sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      ☐ sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.
   b. ☐ *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or tables related thereto, in celectronic form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:

☒	Box No. I	Basis of the report
☐	Box No. II	Priority
☒	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☐	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☐	Box No. VIII	Certain observations on the international application

Date of submission of the demand	Date of completion of this report
24.01.2006	04.04.2006

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INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/GB2004/005053

Box No. I Basis of the report

1. With regard to the **language**, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.

   ☐ This report is based on translations from the original language into the following language , which is the language of a translation furnished for the purposes of:
   - ☐ international search (under Rules 12.3 and 23.1(b))
   - ☐ publication of the international application (under Rule 12.4)
   - ☐ international preliminary examination (under Rules 55.2 and/or 55.3)

2. With regard to the **elements*** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

Description, Pages	
1-56	as originally filed
Claims, Numbers	
1-18	received on 24.01.2006 with letter of 24.01.2006
Drawings, Sheets	
1/7-7/7	as originally filed

   ☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing

3. ☐ The amendments have resulted in the cancellation of:
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

* *If item 4 applies, some or all of these sheets may be marked "superseded."*

Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability

1. The questions whether the claimed invention appears to be novel, to involve an inventive step (to be non-obvious), or to be industrially applicable have not been examined in respect of:

☐ the entire international application,

☒ claims Nos. 1-18

because:

☐ the said international application, or the said claims Nos. relate to the following subject matter which does not require an international preliminary examination (specify):

☐ the description, claims or drawings *(indicate particular elements below)* or said claims Nos. are so unclear that no meaningful opinion could be formed *(specify)*:

☐ the claims, or said claims Nos. are so inadequately supported by the description that no meaningful opinion could be formed.

☒ no international search report has been established for the said claims Nos. 1-18

☐ the nucleotide and/or amino acid sequence listing does not comply with the standard provided for in Annex C of the Administrative Instructions in that:

the written form	☐	has not been furnished
	☐	does not comply with the standard
the computer readable form	☐	has not been furnished
	☐	does not comply with the standard

☐ the tables related to the nucleotide and/or amino acid sequence listing, if in computer readable form only, do not comply with the technical requirements provided for in Annex C-*bis* of the Administrative Instructions.

☒ See separate sheet for further details

Re Item III.

The invention as defined by the originally filed claims 1 - 19, 26 relates to the verification of a processor design. Said verification is performed by running a simulation with two models and comparing the results provided by each of the models. The dependent claims, as originally filed, further specify that the first model is a model of the of the instruction set of the processor while the second model is a model of the hardware implementation of said processor. The dependent claims also specify how the execution of the simulation of the two models is synchronized. Said synchronization is an essential par of the invention, because as indicated in the description (p. 12, first paragraph) the invention is directed to verifying processor designs supporting out of order instruction execution.

The search has been carried out for the **claimed** invention and with due regard to the description and drawings, as required by Article 15(3), Rule 33.3 PCT and the Guidelines (2.02). As a result a plurality of documents relevant to the **claimed** invention were revealed.

The characterising part of claim 1 currently on file, filed with a letter dated 24.01.2006, introduces the step of automatic generation of the instruction set model by compiling the specification. As indicated by the applicant in his letter, accompanying his demand for International Preliminary Examination, the problem solved by the invention is now how to automate the generation of said model.

The newly introduced feature does not have any technical relationship neither with the implementation model nor with the problem of concurrently running the two models and synchronizing their execution. It is even not related to the problem of processor verification, because the model can be used for a plurality of tasks among which system prototyping, specification validation, educational purposes etc.

As there is no technical interaction and therefore no synergetic effect between the newly introduced feature and the other features of claim 1, said claim comprises merely a juxtaposition of features.

And in deed as the problems of running the two models in parallel and automatically

generating an executable model from specification are not technically interrelated, a document disclosing only the compilation of a specification model and not teaching the execution of two different models for verification purposes would, in combination with any of the relevant documents cited in the Search Report, render current claim 1 not inventive. Such a document, however, could not be retrieved by performing the search for the invention **as defined in the original set of claims.**

Therefore the newly introduced feature defines a separate invention which could not have and has not have been searched when performing the search for the originally claimed invention.

Therefore no opinion can be issued regarding the novelty and inventive step of the currently **claimed** subject-matter, because it has not been searched (Rule 70.1(d)).

AMENDED CLAIMS

1. A method of verifying a processor design against a processor specification, the method comprising the steps of

a) creating a verification environment;

b) executing an instruction sequence in a first simulation process within the verification environment, the first simulation process comprising the execution of the instruction sequence according to a representation of the processor specification;

c) executing the instruction sequence in a second simulation process, the second simulation process comprising the execution of the instruction sequence according to a representation of the processor design; and

d) comparing the results of the first simulation with the results of the second simulation within the verification environment in order to verify the processor design,

characterised in that the representation of the processor specification is a machine-executable representation and the method comprises the step of processing the processor specification with a compiler to automatically generate the machine-executable representation of the processor specification for the first simulation process.

2. A method according to any preceding claim, wherein the processor specification comprises a plurality of verifiable elements.

3. A method according to claim 2 wherein, the verification environment maintains the current state of the plurality of verifiable elements.

4. A method according to any preceding claim, wherein the processor specification further comprises a description of any instructions which may be executed by the processor.

5. A method according to claim 4, wherein each said instruction description comprises zero or more actions which define the instruction.

6. A method according to any preceding claim, wherein the processor specification further comprises a description of any stimuli which may cause an exception condition in the processor.

7. A method according to claim 6, wherein each said stimulus description comprises zero or more actions which define the stimulus.

8. A method according to claim 2 or any preceding claim dependent on claim 2, wherein each of the verifiable elements is associated with a respective specification queue, the method comprising the further step of:

executing the actions defining an instruction from the instruction sequence within the first simulation, the execution adding zero or more entries to the specification queue.

9. A method according to claims 7 and 8, the method further comprising the step of executing the actions defining a stimulus, the execution adding zero or more entries to the specification queue.

10. A method according to claim 2, wherein each of the verifiable elements is associated with a respective design queue.

11. A method according to any preceding claim, wherein the verification environment receives one or more notifications from the second simulation, the one or more notifications being generated by the operation of the second simulation.

12. A method according to claim 11 further comprising the steps of:

the verification environment analysing the one or more received notifications; and

the verification environment generating one or more entries in one or more design queue(s) in response to the received notifications.

13. A method according to any preceding claim, further comprising the step of:

the verification environment verifies each verifiable element for which the design queue or the specification queue comprise one or more entries, by comparing the respective queues.

14. A method according to claim 13 wherein the verification environment reports an error if the design queue can not be reconciled with the compared specification queue.

15. A method according to claims 3, 13 and 14 wherein the verification environment:

identifies reconcilable entries within each queue; and

acts on these entries by removing them from the design and specification queues and updating the state of the corresponding verifiable elements.

16. A method according to any preceding claim, wherein the verification environment analyses the processor specification to determine a plurality of processor memory elements.

17. A method according to claim 16, wherein the verification environment further provides memory resources to the second simulation to implement the plurality of processor memory elements.

18. A computer-readable data carrier comprising code for executing a method according to any of the preceding claims.